

1. A method of operating a floating gate pixel, comprising:

providing a P type silicon substrate;

forming an N well in said substrate, wherein said N well is N type silicon and has no contact regions formed therein;

5 forming a P well in said N well, wherein said P well is P type silicon;

forming a contact region in said P well, wherein said contact region is P⁺ type silicon and is the only contact region formed in said P well;

forming a gate oxide on said substrate, wherein said the thickness of said gate oxide is sufficiently small to allow tunneling through said gate oxide;

10 forming a floating gate on said gate oxide, wherein said gate is directly over part of said P well and part of said N well and the only electrical connection to said floating gate is to connect said floating gate to a means for determining the potential of said floating gate;

resetting the potential between said P well and said substrate during a reset period

15 wherein a tunneling current between said P well and said floating gate resets the potential of said floating gate;

accumulating charge at the PN junction between said P well and said N well during a charge integration period, wherein said charge integration period follows said reset period; and

20 reading the potential of said gate after said charge integration period has been completed.

2. The method of claim 1 wherein the charge accumulated at the PN junction between said P well and said N well is related to the amount of light incident on the P well and the N well during said charge integration period.

5 3. The method of claim 1, further comprising:

forming an electrical connection between said contact region formed in said P well and a means for resetting the potential between said P well and said substrate; and

forming an electrical connection between said floating gate and said means for determining the potential of said floating gate.

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4. The method of claim 1 wherein the PN junction between said P well and said N well forms a photodiode.

5. The method of claim 1 wherein the thickness of said gate oxide is less than or equal to

15 30 Angstroms.

6. The method of claim 1 wherein said resetting the potential between said P well and said substrate is accomplished using a reset transistor.

20 7. The method of claim 1 wherein said means for determining the potential of said gate comprises a source follower transistor circuit.

8. A method of operating a floating gate pixel, comprising:

providing an N type silicon substrate;

forming a P well in said substrate, wherein said P well is P type silicon and has no contact regions formed therein;

5 forming an N well in said P well, wherein said N well is N type silicon;

forming a contact region in said N well, wherein said contact region is N⁺ type silicon and is the only contact region formed in said N well;

forming a gate oxide on said substrate, wherein said the thickness of said gate oxide is sufficiently small to allow tunneling through said gate oxide;

10 forming a floating gate on said gate oxide, wherein said gate is directly over part of said N well and part of said P well and the only electrical connection to said floating gate is to connect said floating gate to a means for determining the potential of said floating gate;

resetting the potential between said N well and said substrate during a reset period

15 wherein a tunneling current between said N well and said floating gate resets the potential of said floating gate;

accumulating charge at the PN junction between said N well and said P well during a charge integration period, wherein said charge integration period follows said reset period; and

20 reading the potential of said gate after said charge integration period has been completed.

9. The method of claim 8 wherein the charge accumulated at the PN junction between said N well and said P well is related to the amount of light incident on the N well and the P well during said charge integration period.

5 10. The method of claim 8, further comprising:

forming an electrical connection between said contact region formed in said P well and a means for resetting the potential between said P well and said substrate; and
electrical connection between said floating gate and said means for determining the potential of said floating gate.

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11. The method of claim 8 wherein the PN junction between said P well and said N well forms a photodiode.

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12. The method of claim 8 wherein the thickness of said gate oxide is less than or equal to 30 Angstroms.

13. The method of claim 8 wherein said resetting the potential between said P well and said substrate is accomplished using a reset transistor.

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14. The method of claim 8 wherein said determining the potential of said gate comprises a source follower transistor circuit.

15. A floating gate pixel, comprising:

a P type silicon substrate;

an N well formed in said substrate, wherein said N well is N type silicon and has no contact regions formed therein;

5 a P well formed in said N well, wherein said P well is P type silicon;

a contact region formed in said P well, wherein said contact region is P⁺ type silicon and is the only contact region formed in said P well;

a gate oxide formed on said substrate, wherein said the thickness of said gate oxide is sufficiently small to allow tunneling through said gate oxide;

10 a floating gate formed on said gate oxide, wherein said gate is directly over part of said P well and part of said N well;

means for resetting the potential between said P well and said substrate; and

means for reading the potential of said gate, wherein the only electrical connection to said floating gate is to connect said floating gate to said means for

15 determining the potential of said floating gate.

16. The floating gate pixel of claim 15 further comprising:

electrical connection between said contact region formed in said P well and said means for resetting the potential between said P well and said substrate; and

20 electrical connection between said floating gate and said means for determining the potential of said floating gate.

17. The floating gate pixel of claim 15 wherein the PN junction between said P well and said N well forms a photodiode.

18. The floating gate pixel of claim 15 wherein the thickness of said gate oxide is less
5 than or equal to 30 Angstroms.

19. The floating gate pixel of claim 15 wherein said means for resetting the potential between said P well and said substrate comprises a reset transistor.

10 20. The floating gate pixel of claim 15 wherein said means for determining the potential of said floating gate comprises a source follower transistor circuit.

21. A floating gate pixel, comprising:

an N type silicon substrate;

15 a P well formed in said substrate, wherein said P well is P type silicon and has no contact regions formed therein;

an N well formed in said P well, wherein said N well is N type silicon;

a contact region formed in said N well, wherein said contact region is N⁺ type silicon and is the only contact region formed in said N well;

20 a gate oxide formed on said substrate, wherein said the thickness of said gate oxide is sufficiently small to allow tunneling through said gate oxide;

a floating gate formed on said gate oxide, wherein said gate is directly over part of said N well and part of said P well;

means for resetting the potential between said N well and said substrate; and
means for determining the potential of said gate, wherein the only electrical
connection to said floating gate is to connect said floating gate to said means for
determining the potential of said floating gate.

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22. The floating gate pixel of claim 21 further comprising:

an electrical connection between said contact region formed in said N well and
said means for resetting the potential between said N well and said substrate; and

an electrical connection between said floating gate and said means for
10 determining the potential of said floating gate.

23. The floating gate pixel of claim 21 wherein the PN junction between said N well and
said P well forms a photodiode.

15 24. The floating gate pixel of claim 21 wherein the thickness of said gate oxide is less
than or equal to 30 Angstroms.

25. The floating gate pixel of claim 21 wherein said means for resetting the potential
between said P well and said substrate comprises a reset transistor.

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26. The floating gate pixel of claim 21 wherein said means for reading the potential of
said gate comprises a source follower transistor.